AMENDMENTS TO THE SPECIFICATION

Please replace subtitle 1 on page 1 with the following amended subtitle:

Technical Field ~~of the Invention~~

Please replace paragraph 0001 with the following amended paragraph:

[0001] ~~The invention relates to a~~ A method of manufacturing a semiconductor device is disclosed, ~~and more particularly, to a method of manufacturing a semiconductor device~~ which is capable of preventing a transient enhanced diffusion (TED) phenomenon generated ~~on~~ by ions of a well region as well as maintaining activation of ions implanted on the well region to the maximum extent when forming the well area.

Please replace subtitle 2 on page 1 with the following amended subtitle:

Discussion of the Related Art

Please replace paragraph 0003 with the following amended paragraph:

[0003] In particular, ions are implanted into an active region for forming a well region before a floating gate of a flash memory device is formed, and the ions for forming a well region must minimize the damage ~~of~~ to a semiconductor substrate generated from an ion implantation process performed at high energy and maintain activation ratio of ions implanted into the well region (that is, coupling strength between ~~ion~~ ions implanted into a semiconductor substrate and the silicon of the substrate).

Please replace paragraph 0004 with the following amended paragraph:

But, the ions formed in a well region so as to satisfy conditions mentioned above become diffused into another film, for example, an oxide film of a element isolation film due to the high-temperature heat treatment process to be performed later ~~and therefore~~ thereby causing the TED phenomenon ~~is brought out~~.

Please replace the title on page 2 with the following amended title:

SUMMARY OF THE ~~INVENTION~~ DISCLOSURE

Please replace paragraph 0005 with the following amended paragraph:

[0005] ~~The present invention is contrived to~~ To solve the above problems, ~~and the present invention is thus directed to~~ a method of manufacturing a semiconductor device is disclosed which is capable of maintaining activation of ions implanted ~~on~~ into the well region to the maximum extent when forming the well area, minimizing the damage of a semiconductor substrate when performing an ion implantation process, and preventing transient enhanced diffusion (TED) phenomenon generated on ions of a well region.

Please replace paragraph 0006 with the following amended paragraph

[0006] One ~~aspect of the present invention is to provide a~~ disclosed method of manufacturing a semiconductor device~~, comprising the steps of:~~ comprises forming a first well region by performing an ion implantation process for implanting first ions into a semiconductor substrate, and then forming a second well region in the first well region by performing an ion implantation process for implanting second ions having larger mass than the first ions; and forming a three-fold well region by performing an annealing process on the ~~result~~ resultant structure wherein the lighter first ions are disposed in the upper and lower well regions and the heavier second ions are disposed in the middle well region.

Please replace paragraph 0007 with the following amended paragraph:

[0007] ~~In the aforementioned of a method of manufacturing a semiconductor device according~~ According to another ~~embodiment of the present invention~~ refinement, the first well region is formed by implanting phosphorus (P) ions at a tilt angle of 3° to 13° with a dose in the range of 1E11 ions/cm^2 to 1E14 ions/cm^2 at an energy of about 500 KeV to 3000KeV, by using a high-energy ion implantation device.

Please replace paragraph 0008 with the following amended paragraph:

[0008] ~~In the aforementioned of a method of manufacturing a semiconductor device according~~ According to another ~~embodiment of the present invention~~ refinement, the second well region is formed by implanting arsenic (As) ions having larger mass than phosphorus ions, at a tilt angle of 3° to 13° with a dose of 1E11 ions/cm^2 to 1E14 ions/cm^2 at an energy of about 100 KeV to 300KeV, by using a middle-current ion implantation device.

Please replace paragraph 0009 with the following amended paragraph:

[0009] ~~In the aforementioned of a method of manufacturing a semiconductor device according~~ According to another ~~embodiment of the present invention~~ refinement, the annealing process is performed using one of an RTP process performed under N_2 or H_2 gas atmosphere at a temperature of 900°C to 1000°C for ~~10seconds~~ 10 seconds to 60 seconds, or a furnace process performed under N_2 or H_2 gas atmosphere at a temperature of 900°C to 1100°C for ~~10minutes~~ 10 minutes to 60 minutes.

Please replace paragraph 0010 with the following amended paragraph:

[0010] ~~In the aforementioned of a method of manufacturing a semiconductor device according~~ According to another ~~embodiment of the present invention~~ refinement, ~~further comprising the steps of~~ the method comprises forming a region into which ions for adjusting a threshold voltage are implanted on the semiconductor substrate on which well regions are formed, and then forming a tunnel oxide film, a floating gate electrode, a dielectric film and a control gate electrode on an upper part of the semiconductor substrate.

Please replace paragraph 0011 with the following amended paragraph:

[0011] ~~In the aforementioned of a method of manufacturing a semiconductor device according~~ According to another ~~embodiment of the present invention~~ refinement, ~~further comprising a step of~~ the method comprises forming a screen oxide film serving as a buffer layer for suppressing a damage generated by the ion implantation process for forming the first well region and the second well region before forming the well region.

Please replace paragraph 0012 with the following amended paragraph:

[0012] The ~~aforementioned aspects and other~~ Other features of the ~~present invention~~ disclosed methods will be explained in the following description, taken in conjunction with the accompanying drawings, wherein:

Please replace paragraph 0013 with the following amended paragraph:

[0013] Figs. 1 to 4 are views illustrating a method of forming a well region of a semiconductor device according to a preferred embodiment ~~of the present invention~~.

Please replace the title on page 4 with the following amended title:

DETAILED DESCRIPTION OF THE PRESENTLY PREFERRED EMBODIMENTS

Please replace paragraph 0014 with the following amended paragraph:

[0014] The ~~present invention~~ disclosed methods will be described in detail by way of following preferred embodiments with reference to accompanying drawings. But, the following preferred embodiments can be modified into other embodiments within the scope of ~~the present invention~~ this disclosure by those having ordinary skill in the art and access to the teachings of ~~the present invention~~ this disclosure, and therefore the scope of ~~the present invention~~ this disclosure is not limited to the following embodiments. In the following explanation, thickness of a particular layer, etc., in the figures are blown up for convenience and clearness of explanation, and like reference numerals in the figures are used to identify the same or similar parts. Also, an expression that one layer exists on another layer or on a semiconductor substrate means that one layer may exist on the very another layer or on the semiconductor substrate, or other layer may lie between one layer and another layer or a semiconductor substrate.

Please replace paragraph 0015 with the following amended paragraph:

[0015] Figs. 1 to 4 are views illustrating a method of forming a well region of a semiconductor device according to a preferred embodiment ~~of the present invention~~.

Please replace paragraph 0016 with the following amended paragraph:

[0016] Referring to Fig. 1, a screen oxide film 12 is formed on a front of an upper part of a semiconductor substrate 10. The semiconductor substrate 10 is divided into a region where p-channel transistor is formed (hereafter "PMOS region") and a region where n-channel transistor is formed (hereafter "NMOS region"). A method of forming a well region of the PMOS region is explained ~~specifically in the present invention~~.

Please replace paragraph 0018 with the following amended paragraph:

[0018] Referring to Fig. 2, a first ~~well~~ region 14 defines a well region and is formed by forming a photoresist pattern (PR) on a predetermined region of the result structure and then performing ~~an~~ a first ion implantation process on the semiconductor substrate 10 using the PR as a mask for implanting ions.

Please replace paragraph 0019 with the following amended paragraph:

[0019] At this time, the ion implantation process ~~for forming the first well region 14~~ is performed by implanting phosphorus (P) ions at a tilt angle of 3 to 13°, at a dose of 1E11 to 1E14 ions/cm^2, and to form the first region 14 at the energy of about 500 to 3000KeV using a high-energy ion implantation device

Please replace paragraph 0020 with the following amended paragraph:

[0020] Referring to Fig. 3, a second ~~well~~ region 16 is formed by performing ~~an~~ a second ion implantation process on the first ~~well~~ region 14 using the PR as a mask for implanting ions. At this time, the ion implantation process for forming the second ~~well~~ region 16 is performed by implanting arsenic (As) ions (size 75) having larger mass than phosphorus ions (size 31), which form the first ~~well~~ region 14 , at the tilt angle of 3 to 13° with a dose of 1E11 to 1E14 ions/cm^2 at the energy of about 100 to 300KeV using a middle-current ion implantation device. Then, a process of eliminating the PR is performed.

Please replace paragraph 0021 with the following amended paragraph:

[0021] Referring to Fig. 4, when an annealing process is performed on the front of the result structure, a ~~threefold~~ three-fold well region 14a/16a/14b having a first well region 14a implanted primarily with the first ions, a second well region 16a implanted primarily with the second ions and a third well region 14b implanted primarily with the first ions. The annealing results in the migration of the heavier and lighter ions into the three part well region 14a/16a/14b as shown in Fig. 4 with the heavier ions in the middle well region 16b and the lighter ions in the top and bottom well regions 14b, 14a ~~where the second well region 16 is interposed between the first well regions 14 is formed~~. When an annealing process is performed after the first ~~well~~ region 14 and the second ~~well~~ region 16 are formed (see Fig. 3), the ion density of ~~a source/drain~~ the region is increased. Then, the increase of

the ion density of ~~a source/drain~~ the well region makes it possible to prevent TED phenomenon generated due to the high-energy heat treatment process to be performed later such as an oxidation process by decreasing the diffusion speed of the implanted ions. Because ions having large mass and ions having small mass are implanted into same region and mixed, the activation ratio of ions is increased compared with the conventional ~~source/drain~~ well region in which only the ions having large mass are implanted.

Please replace paragraph 0022 with the following amended paragraph:

[0022] Also, it is possible to compensate for the damage of the semiconductor substrate generated in the ion implantation process performed at high energy for forming the first and the second ~~well~~ regions and the damage of the semiconductor substrate generated due to implantation of ions having large mass by performing said annealing process.

Please replace paragraph 0023 with the following amended paragraph:

[0023] A rapid thermal process (RTP) annealing process or a furnace annealing process may be used as the annealing process mentioned above. The RTP annealing process is performed under N_2 or H_2 gas atmosphere at a temperature of 900 to 1000°C for 10 to 60 seconds, and the furnace annealing process is performed under N_2 or H_2 gas atmosphere at a temperature of 900 to 1100°C for 10 to 60 minutes. ~~A~~ The screen oxide film 12 is removed after the annealing process.

Please replace paragraph 0025 with the following amended paragraph:

[0025] According to ~~the~~ an embodiment ~~of the present invention~~, it is possible to prevent TED phenomenon generated due to the high-energy heat treatment process to be performed later such as an oxidation process and to provide the increased activation ratio of ions compared with the conventional source/drain region in which only the ions having large mass are implanted by performing an annealing process after the first well region and the second well region are formed.

Please replace paragraph 0027 with the following amended paragraph:

[0027] Although the foregoing description has been made with reference to the preferred embodiments, it is to be understood that changes and modifications ~~of the present invention~~ may be made by the ordinary skilled in the art without departing from the spirit and scope of the ~~present invention and~~ appended claims.

Please replace paragraph 0028 with the following amended paragraph:

[0028] It is therefore intended by the appended claims to cover any and all such changes and modifications ~~within the scope of the present invention~~.